



SAMR21 Xplained Pro PCB Specification



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1 General information

1.1 Board identification

Name: SAMR21 Xplained Pro

Board identification number: A08-1903, rev1

1.2 Contact persons for PCB issues.

- PCB Designer: Are Halvorsen, are.halvorsen@atmel.com, +47 72 89 75 18
- PCB Designer: Lars Häring, lars.haring@atmel.com, +47 911 307 58

2 PCB specification

2.1 Manufacturing data

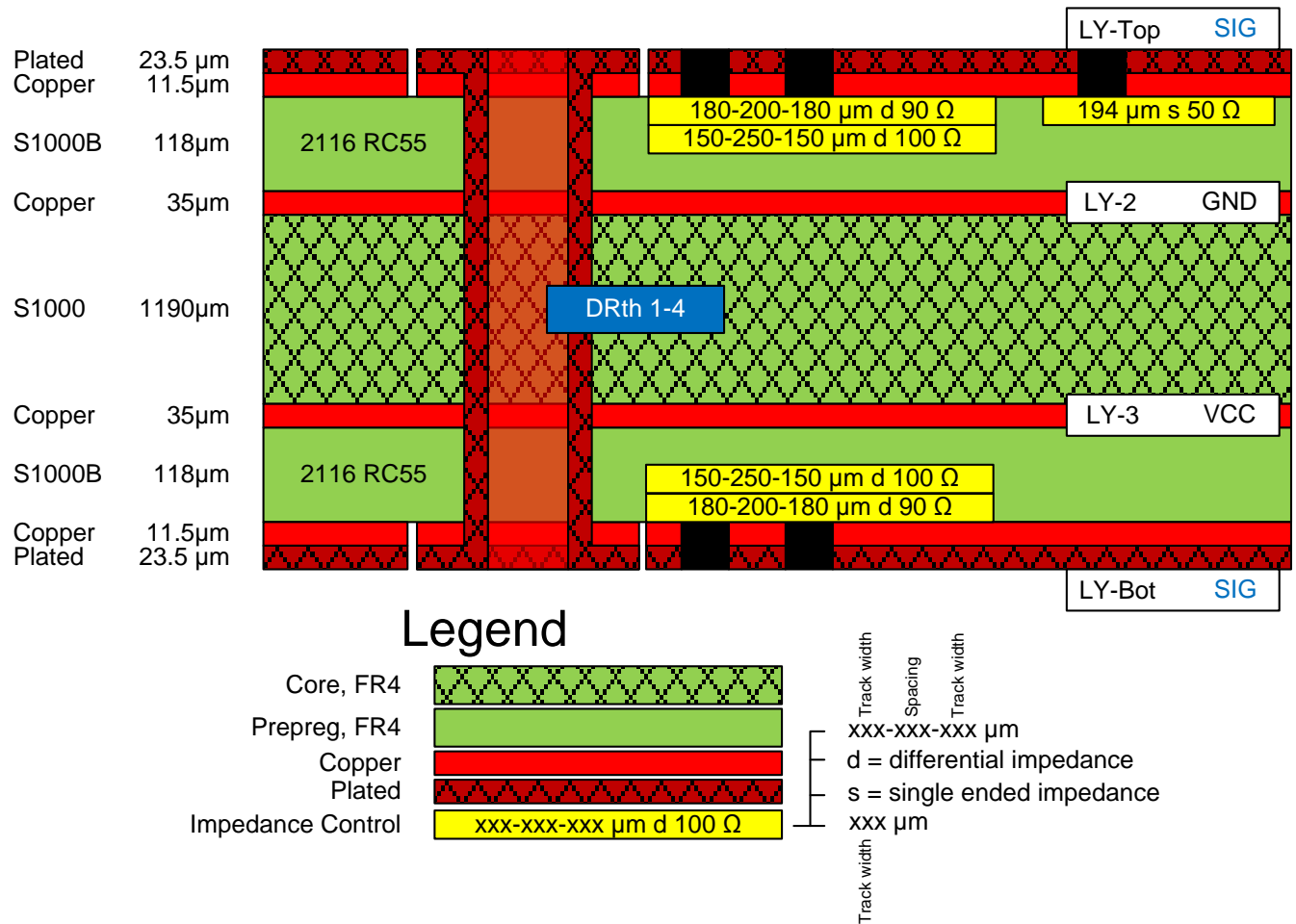
- Size: 60mm x 60mm
- PCB material: S1000, 1.6mm thickness
- Layers: 4
- Finish: ENIG
- Minimum via hole size: 0.2 mm
- Minimum via pad size: 0.4 mm
- Minimum track width: 0.125 mm (4.9mil)
- Minimum spacing: 0.12 mm (4.6mil)
- Solder mask color: Dark BLUE
- Silk-screen color: White



2.2 Layer stack-up

Figure 2-1 shows the detailed layer stack-up for this PCB.

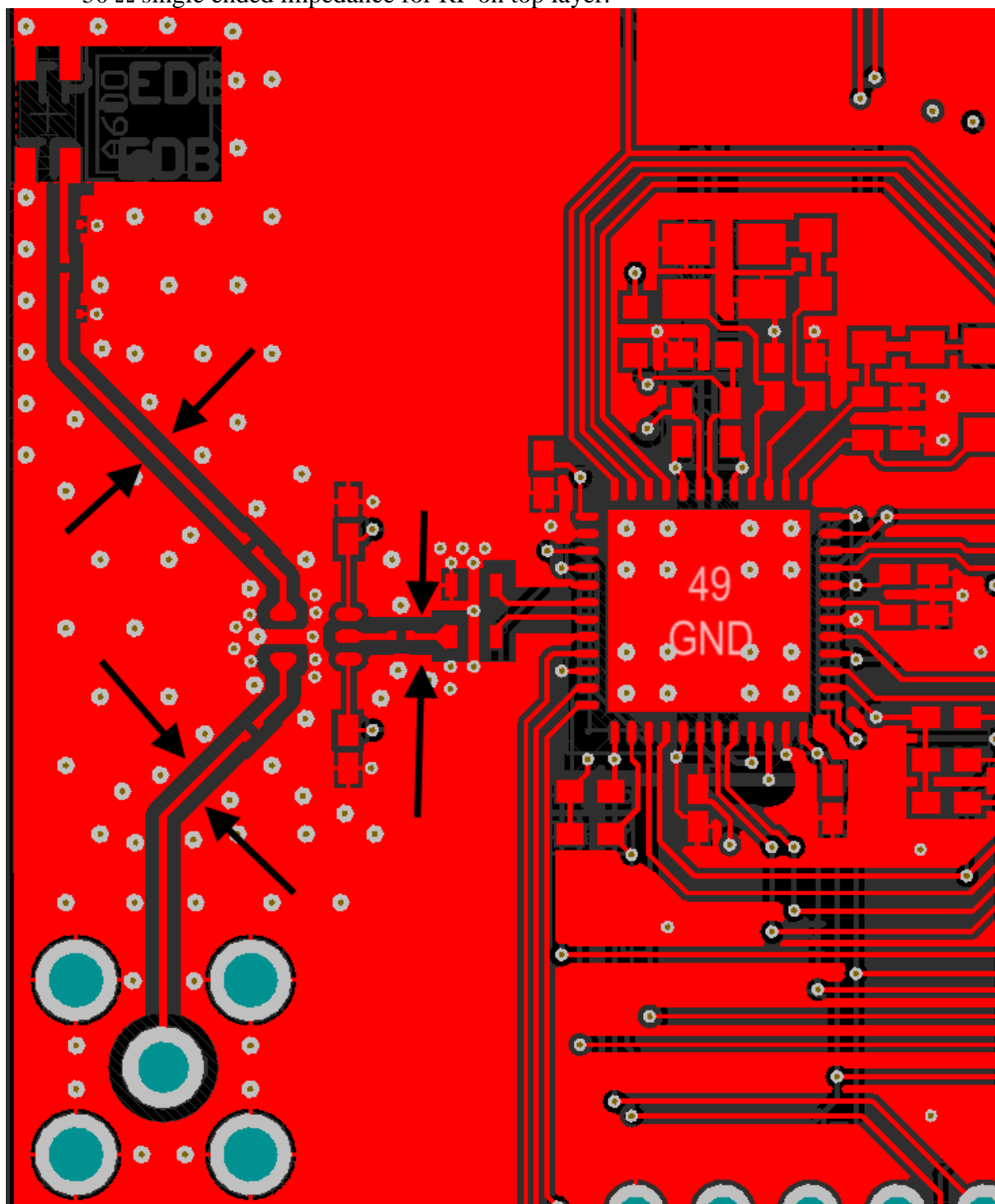
Figure 2-1 Detailed layer stack-up



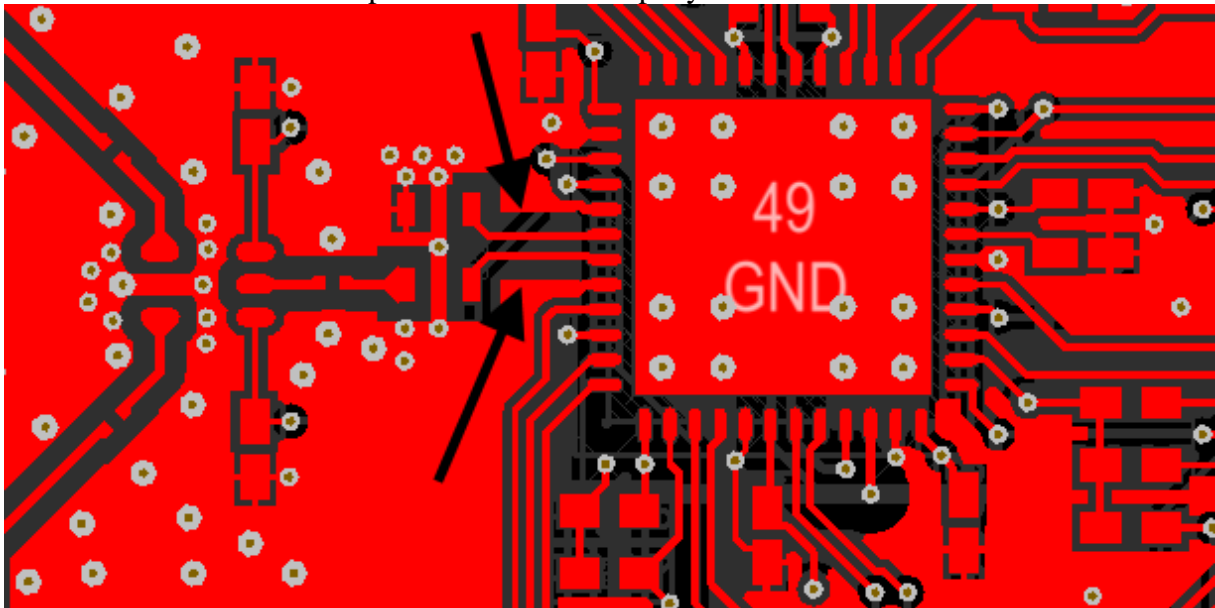
2.3 Controlled Impedance

This board required three different controlled impedances.

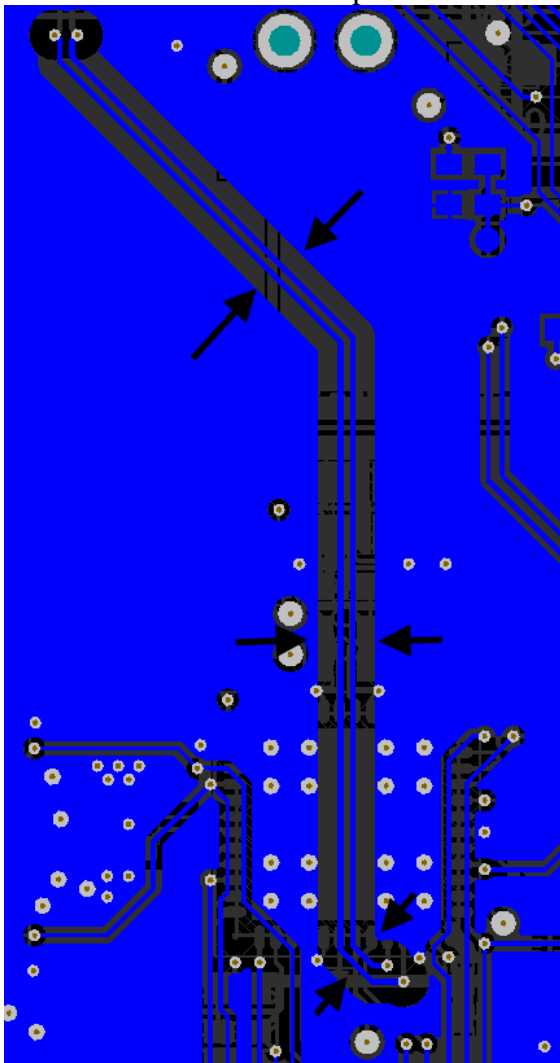
- 50 Ω single ended impedance for RF on top layer.



- 100 Ω differential impedance for RF on top layer.



- 90 Ω differential impedance for USB on bottom layer.





2.4 Gerber files

Table 2-1 Layer stackup corresponding Gerber files (listed from top to bottom)

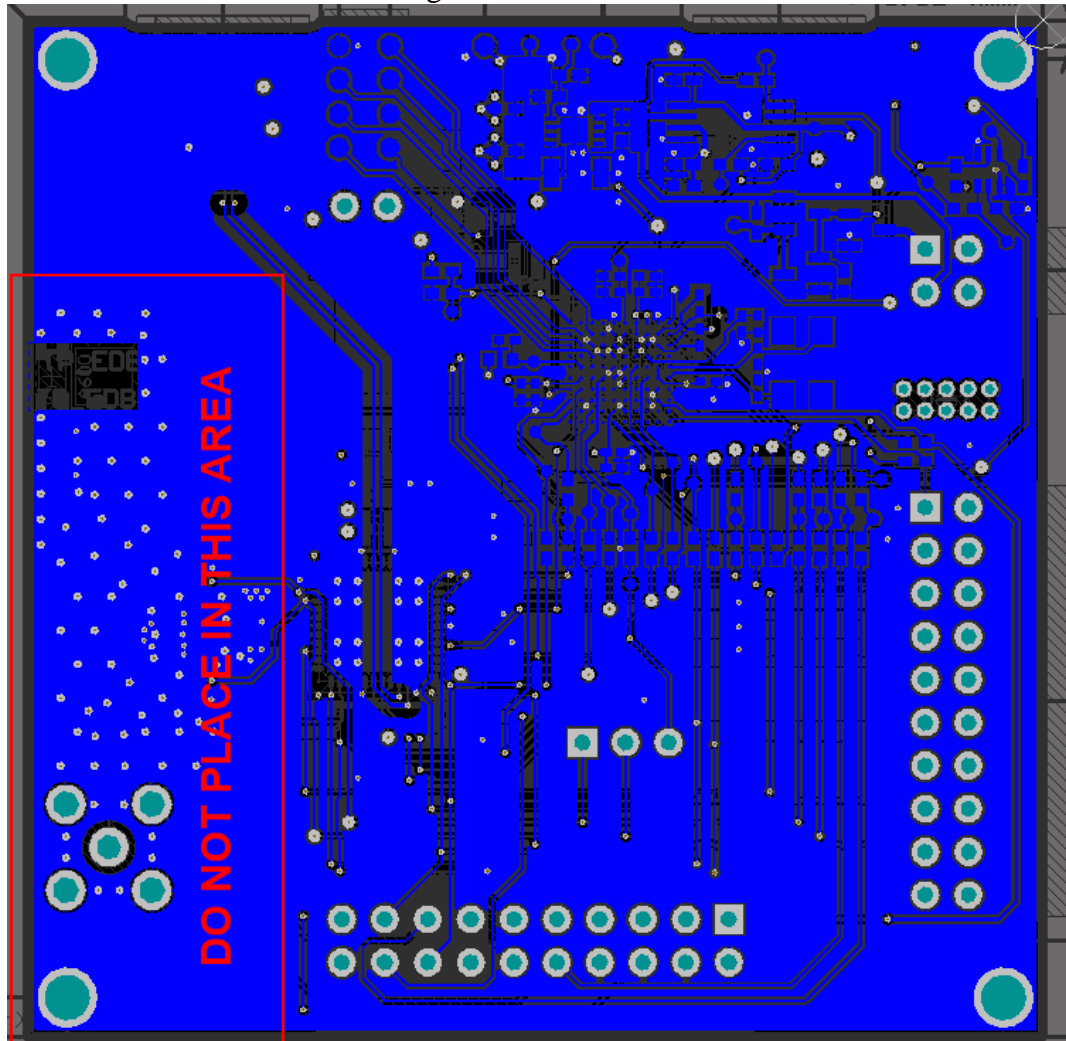
File name	Description
SAMR21_Xplained_Pro.GTP	Gerber file for top paste-mask
SAMR21_Xplained_Pro.GTO	Gerber file for top overlay (silkscreen)
SAMR21_Xplained_Pro.GTS	Gerber file for top solder-mask
SAMR21_Xplained_Pro.GTL	Gerber file for top layer
SAMR21_Xplained_Pro.GP1	Gerber file for internal plane layer 1 (GND layer)
SAMR21_Xplained_Pro.GP2	Gerber file for internal plane layer 2 (power layer)
SAMR21_Xplained_Pro.GBL	Gerber file for bottom signal layer
SAMR21_Xplained_Pro.GBS	Gerber file for bottom solder-mask
SAMR21_Xplained_Pro.GBO	Gerber file for bottom overlay (silkscreen)
SAMR21_Xplained_Pro.GBP	Gerber file for bottom paste-mask
SAMR21_Xplained_Pro.GM1	Gerber file for mechanical 1 layer (board outline)
SAMR21_Xplained_Pro.DRR	Drill file report
SAMR21_Xplained_Pro.TXT	Drill file

2.5 Special via considerations

All vias are covered with soldermask on the top side of the board. On the bottom side vias that are used as testpoints have openings in the soldermask.

2.6 Placement of fabrication ID mark

The fabrication ID mark should be placed on the bottom side, do **not** place the fabrication ID in the outlined area in the drawing.



3 Panelizing

When making panels for this board the following issues should be considered.

- Fiducial marks should be placed on the panel.

4 Quality of silkscreen layers

The silkscreen layers for the PCB must be of high quality for several reasons:

- Very small text is used
- Text is close to pads and therefore the mask must be centered properly on the board
- The PCB is used for development boards and therefore the silkscreen is an essential part of the overall product quality.