AN-1370
APPLICATION NOTE

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Design Implementation of the ADF7242 Pmod Evaluation Board Using the Johanson Technology, Inc., 2450AT18A100 Chip Antenna

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INTRODUCTION

Due to the continuous innovation of technology in radio frequency (RF) communications, many new designs feature a small form factor 2.4 GHz band wireless module connectivity. This application note describes the use and design implementation of the EVAL-ADF7242-PMDZ, a 2.4 GHz wireless transceiver peripheral module (Pmod™) evaluation board that uses an ADF7242 transceiver in conjunction with a Johanson 2450AT18A100 chip antenna. The chip antenna makes the ADF7242 evaluation board more compact, more cost effective, and easier to use. This application note includes printed circuit board (PCB) layout considerations and simulations used to achieve the optimum performance of the ADF7242 with a given amount of power.

The ADF7242 is an Analog Devices, Inc., low power transceiver IC that operates in a 2400 MHz to 2483.5 MHz industrial, scientific, and medical (ISM) band. It is an extensive, integrated transceiver solution with excellent performance that is suitable for numerous wireless network applications. The ADF7242 has two differential RF ports (RFIO1 and RFIO2) that support antenna diversity and features programmable data rates, modulation, and an output power up to 3 dBm. For the complete specifications of the ADF7242, consult the ADF7242 data sheet.

The ADF7242 has an existing evaluation board, the EVAL-ADF7242DB1Z, which uses a whip antenna in conjunction with its motherboard, the EVAL-ADF7XXXMB3Z. The design of the EVAL-ADF7242-PMDZ provides simple and suitable programming interface connections between the ADF7242 and the host microcontroller with the use of a Pmod connector. This allows the customer to use the ADF7242 in various applications. Applications of a 2.4GHz wireless transceiver include ZigBee, home automation, consumer electronics, monitoring, and remote control. Transforming the EVAL-ADF7242DB1Z into a low cost, 0.8 in wide, small profile EVAL-ADF7242-PMDZ makes it more compact and easier to use without degrading performance.

The EVAL-ADF7242-PMDZ is a flexible and accessible solution because it supports RF to field-programmable gate array (FPGA) or processor applications systems that use Pmod-compatible expansion ports configurable for serial port interface (SPI).

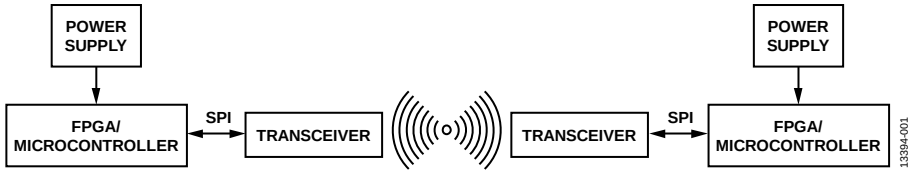

Figure 1. Typical Application Interface System

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REVISION HISTORY

11/15—Revision 0: Initial Version

CHIP ANTENNA DESCRIPTION

A chip antenna is a quarter wave monopole antenna that works with a printed circuit board (PCB) ground plane to form a dipole system. The 2450AT18A100 Johanson Technology mini 2.45 GHz antenna, a 3.2 mm × 1.6 mm ceramic surface-mount element, was used in this circuit. Consult the antenna data sheet when designing the PCB layout. The data sheet contains thorough layout specifications, including mounting considerations with or without matching circuits, ground plane clearance, and a controlled impedance feed line with matching circuits.

Because it is difficult to have a perfect 50 Ω coplanar waveguide or feed line between the RF front end and the antenna, include a pi-matching network or a T-matching network before the chip antenna. This also allows tuning of the antenna to operate at the desired operating frequency and to obtain optimum performance. Achieve maximum power transfer to the chip antenna by combining a 50 Ω controlled impedance trace and a precise matching circuit.

Antenna Specifications

Table 1 details the specifications of the 2450AT18A100 chip antenna.

Table 1. Johanson 2450AT18A100 Chip Antenna

Parameter	Value
Frequency Range	2400 MHz to 2500 MHz
Peak Gain	0.5 dBi typical (XZ-V)[1]
Average Gain	−0.5 dBi typical (XZ-V)[1]
Return Loss	9.5 dB minimum
Input Power	2 W maximum continuous wave
Impedance	50 Ω
Operating Temperature Range	−40°C to +125°C

[1] XZ-V means XZ vertical.

Mechanical Dimensions

Figure 2 shows the mechanical dimensions of the chip antenna.

	INCHES	MILLIMETERS
L	0.126 ± 0.008	3.20 ± 0.20
W	0.063 ± 0.008	1.60 ± 0.20
T	0.051 + 0.004/–0.008	1.30 + 0.1/–0.2
a	0.020 ± 0.012	0.50 ± 0.30

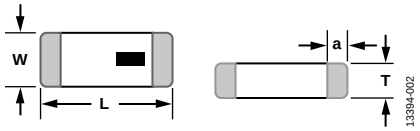

Figure 2. Mechanical Dimensions

Mounting Considerations

Figure 3 shows mounting considerations for the chip antenna.

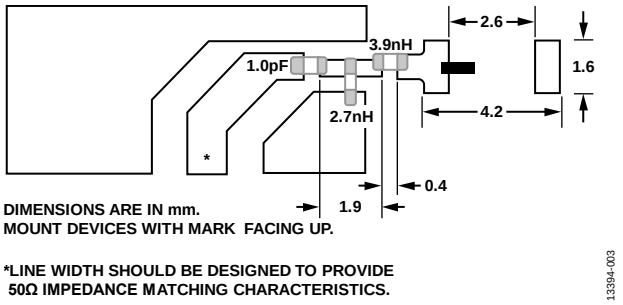

Figure 3. Mounting Considerations

Antenna Performance

The specifications of the 2450AT18A100 chip antenna detailed in Table 1 and the antenna performance and characteristics shown in Figure 2 and Figure 3 originate from the antenna data sheet. The chip antenna is owned by Johanson Technology Inc., an independent corporation that is not owned by, controlled by, or an affiliate of Analog Devices. Analog Devices makes no representations or warranties with respect to the Johanson 2450AT18A100 or any other Johanson Technology products.

Figure 4, Figure 5, and Figure 6 originate from the 2450AT18A100 chip antenna data sheet. They show the actual performance of the chip antenna when used with a Johanson Technoloy evaluation board. Performance results of the chip antenna differ depending upon the evaluation board on which the antenna is used.

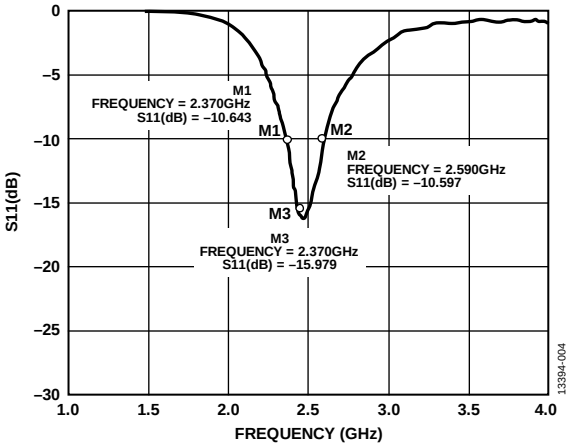

Figure 4. Return Loss with Matching Circuit at 25°C

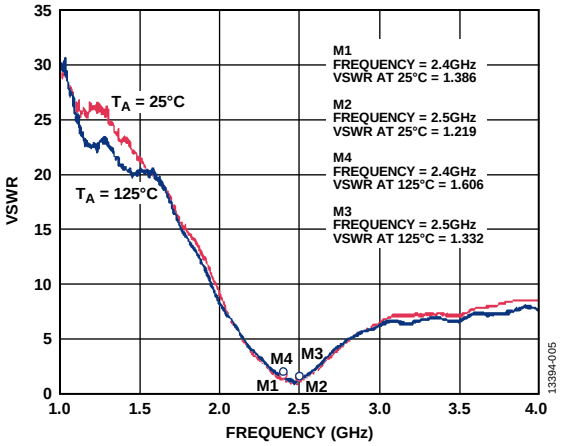

Figure 5. VSWR with Matching Circuit at 25°C and 125°C

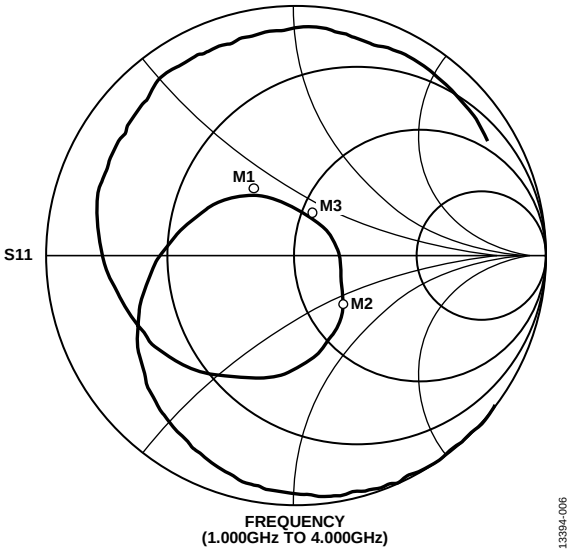

Figure 6. S11 on a Smith Chart

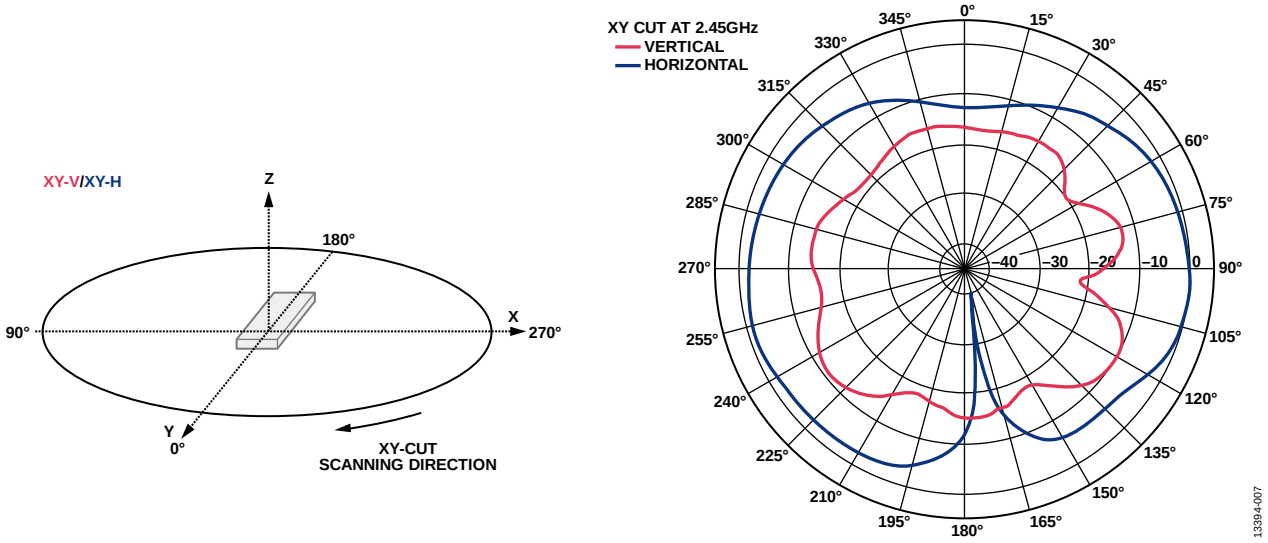

Figure 7. 2450AT18A100 Chip Antenna Typical Radiation Pattern, XY Cut at 2.4 GHz (25°C)

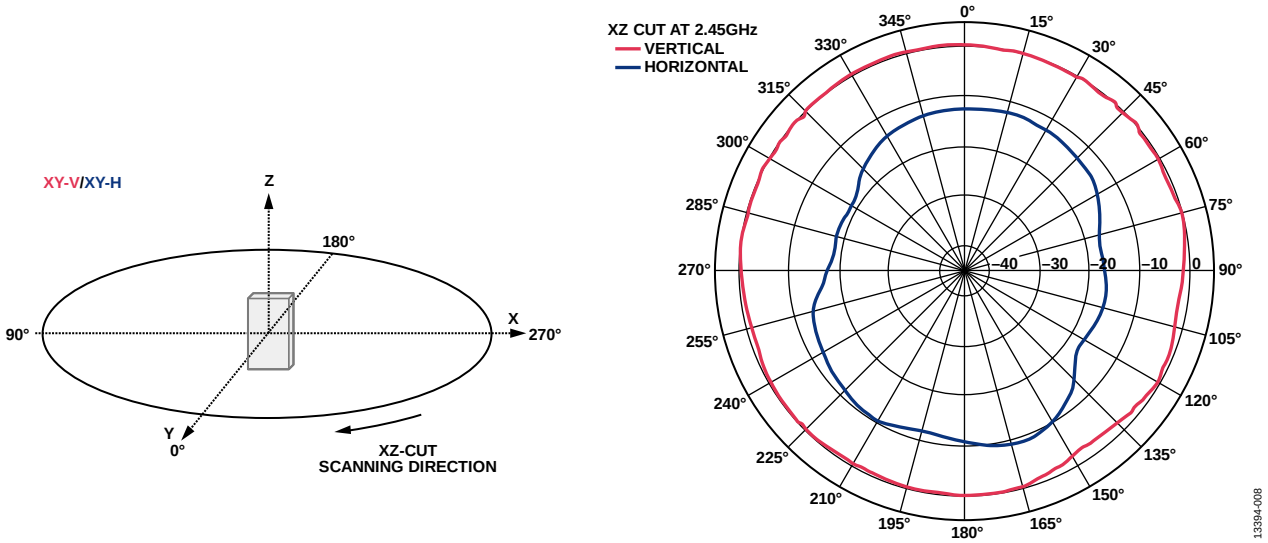

Figure 8. 2450AT18A100 Chip Antenna Typical Radiation Pattern, XZ Cut at 2.4 GHz (25°C)

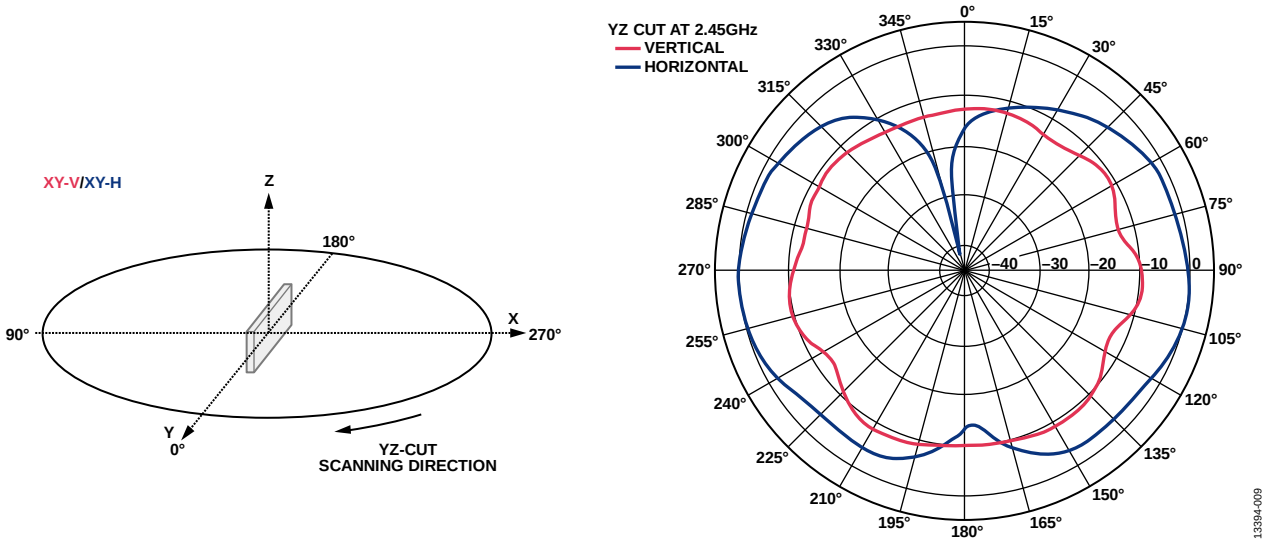

Figure 9. 2450AT18A100 Chip Antenna Typical Radiation Pattern, YZ Cut at 2.4 GHz (25°C)

EVALUATION BOARD SCHEMATIC DESIGN

The EVAL-ADF7242-PMDZ hardware consists of the ADF7242 2.4 GHz low power transceiver with an SPI communication interface (Pmod), baluns, matching circuits, and RF chip antennas. The board is directly powered via the 3.3 V power supply from the Pmod connector with a very low power consumption in both receive and transmit modes.

The differential RF port includes a 10 nF coupling capacitor required as specified in the data sheet. For the transmitter section, the ADF7242 has an optimum power amplifier (PA) with a matching impedance of 43.7 + 35.2j Ω at a maximum output power of 3 dBm. For the receiver section, it has a low noise amplifier (LNA) with input impedance at the RFIO1 port of 50.2 – 52.2j Ω and RFIO2 port of 74.3 – 10.7j Ω. An impedance matched filter balun developed by Johanson Technology matches those impedances to the antenna source impedance of 50 Ω. The balun also performs a single-ended to differential conversion function. Right after the 50 Ω unbalanced port of the filter balun, implement a pi-matching circuit to properly tune the chip antenna and obtain optimum antenna performance. For proper layout guidelines, see the Evaluation Board Layout section of this application note.

Figure 10 shows the EVAL-ADF7242-PMDZ hardware and Figure 11 shows the simplified connection circuit between the ADF7242 and the chip antenna.

Figure 10. EVAL-ADF7242-PMDZ Hardware

GENERAL SPECIFICATIONS

Table 2 shows the typical performance of the EVAL-ADF7242-PMDZ evaluation board achieved at V_{DD} = 3.3 V, T_A = 25°C, $f_{CHANNEL}$ = 2450 MHz, RFIO2 port.

Table 2. Typical Performance of the EVAL-ADF7242-PMDZ Using the 2450AT18A100 Chip Antenna

Parameter	Value
Output Power	3 dBm
Transmission Range	100 m at 250 kbps
Current Consumption	19 mA (Rx mode)
	21.5 mA (Tx mode, P_O = 3 dBm)

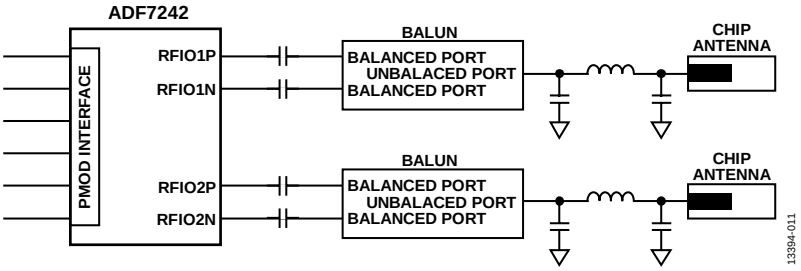

Figure 11. Simplified Connection Circuit Between the ADF7242 and the Chip Antenna

EVALUATION BOARD LAYOUT

Figure 12 shows the PCB layout of the EVAL-ADF7242-PMDZ, emphasizing the location of two orthogonally mounted chip antennas (FL1 and FL2). This layout uses the dual differential RF port interface of the ADF7242, which is configurable for antenna diversity. The Gerber files of the board layout are available for download at www.analog.com/EVAL-ADF7242-PMOD.

The EVAL-ADF7242-PMDZ is a Pmod form factor based on Pmod interface specifications from Digilent. Table 3 details the standard pinouts for a 12-pin connector.

Table 3. Pmod Interface Connector (P1) Signal Descriptions (SPI Communications)

Pin Number	Signal	Description
1	CS	Chip select
2	SDI	Serial data in
3	SDO	Serial data out
4	SCLK	Serial clock
5	GND	Power supply ground
6	VCC	Power supply (3.3 V)
7	IRQ1	Interrupt request output 1
8	NC	Not connected
9	IRQ2	Interrupt request output 2
10	NC	Not connected
11	GND	Power supply ground
12	VCC	Power supply (3.3 V)

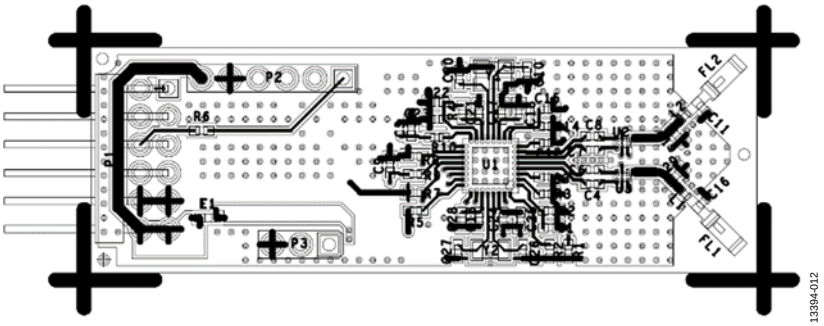

Figure 12. EVAL-ADF7242-PMDZ Board Layout Highlighting the Chip Antenna Placement

PCB LAYOUT CONSIDERATIONS

For optimum performance between the RF path and the chip antenna, consider the following when designing the PCB layout:

- The EVAL-ADF7242-PMDZ uses a balun filter for impedance matching and the conversion function from single-ended to differential. The balun requires vias at its ground pins.
- Ground the stitching around the edges of the board to eliminate coupling and slot radiation.
- Place the regulator capacitors and decoupling capacitors as close as possible to the transceiver IC.
- Design the PCB traces carefully to match the 50 Ω impedance of the antenna. The impedance of the PCB traces depends on the dielectric constant of the PCB material, trace width, and the height above the ground plane.
- The chip antenna must be free from the surrounding ground planes at the distance specified on the 2450AT18A100 chip antenna data sheet.
- Ensure that the PCB trace from the balun to the antenna is as short as possible.
- Place the pi-matching circuit at a close proximity and specific distance to the chip antenna.
- Properly mount the chip antenna as specified on the 2450AT18A100 chip antenna data sheet.

PCB LAYOUT SIMULATIONS

When designing an RF PCB layout, use simulations to validate that the PCB layout does not affect the performance of the RF path. The use of the pi-matching circuit on the actual evaluation board is necessary to match the PCB trace to 50 Ω, which is the center of the Smith chart at the desired frequency.

The PCB layout simulation used the Keysight Advanced Design System (ADS) simulation tool to completely characterize and optimize the PCB design. The simulation occurs from the RF differential ports of the ADF7242 up to the chip antenna.

Figure 14 shows the simulation equivalent schematic set up. Each block in the schematic contains the extracted S-parameter file for each trace shown in Figure 15 to Figure 17 using the ADS simulation tool. Also included in the schematic is the S-parameter file of each RF front-end component used, taken from manufacturers of the specific components.

Figure 13 shows the FR-4 substrate material of the EVAL-ADF7242-PMDZ PCB evaluation board.

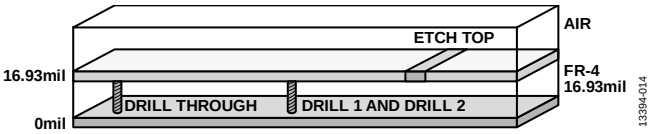

Figure 13. EVAL-ADF7242-PMDZ Substrate Material

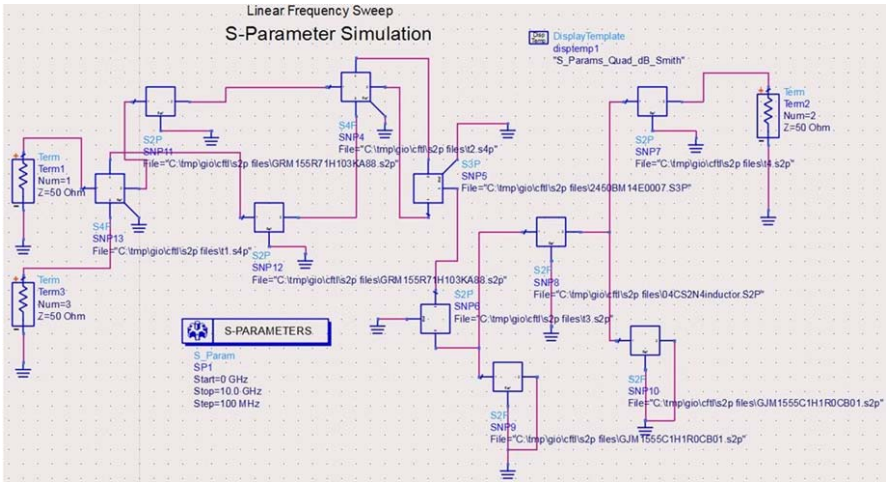

Figure 14. Simulation Equivalent Schematic

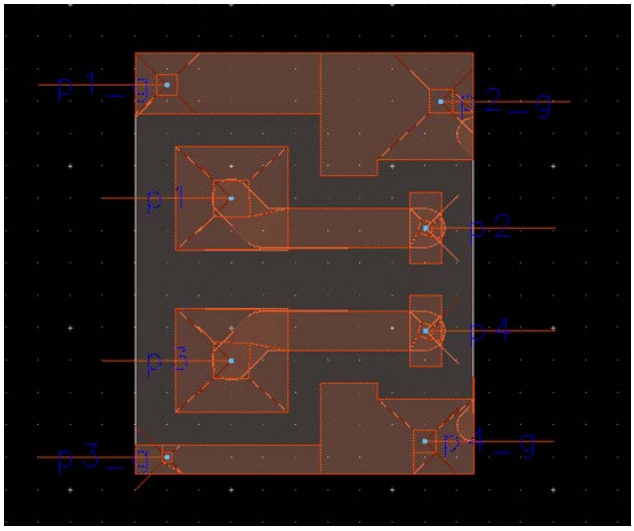

Figure 15. Trace from Decoupling Capacitor to Balun Balanced Port

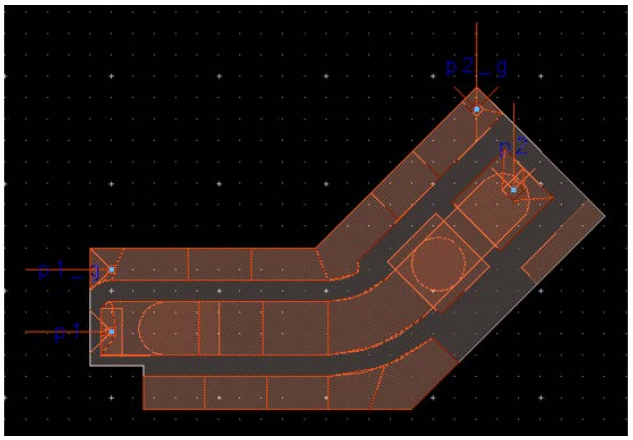

Figure 16. Trace from Balun Unbalanced Port to Matching Circuit

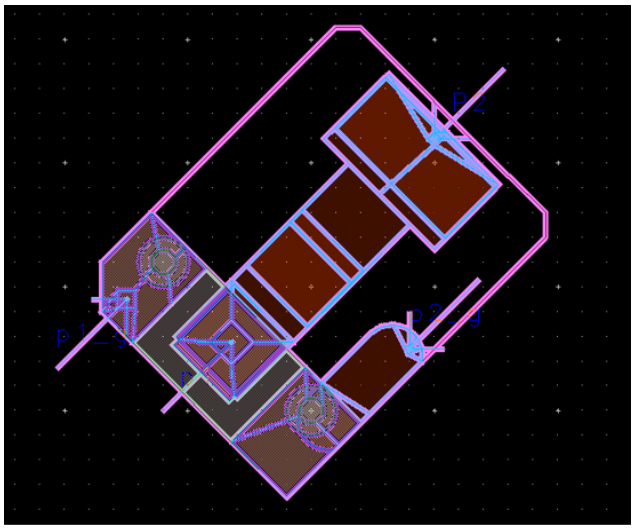

Figure 17. Trace from Matching Circuit to Chip Antenna

PCB LAYOUT SIMULATION RESULTS

Figure 18 and Figure 19 show the results from simulations performed on the ADS. The S-parameters describe the performance of the RF path in terms of the power transfer, gain, losses, and frequency response.

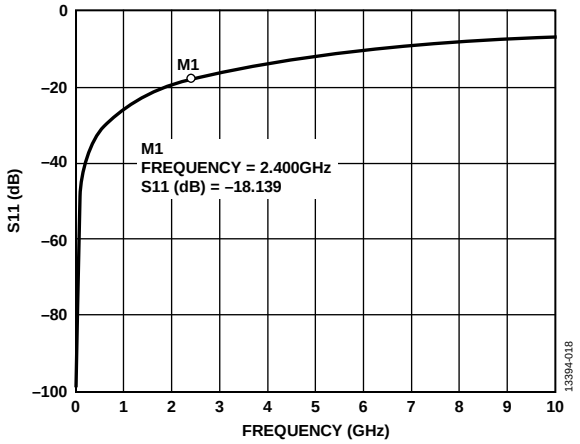

Figure 18. Return Loss

Return loss characterizes the amount of power reflected from the feed line and is a commonly valued parameter for the antenna. It is usually displayed as S11 in dB. Figure 19 indicates that the RF radiates at 2.400 GHz, with S11 = −18.139 dB. It is more efficient than the acceptable return loss of −10 dB to −15 dB and reflects only 1.58% of the power.

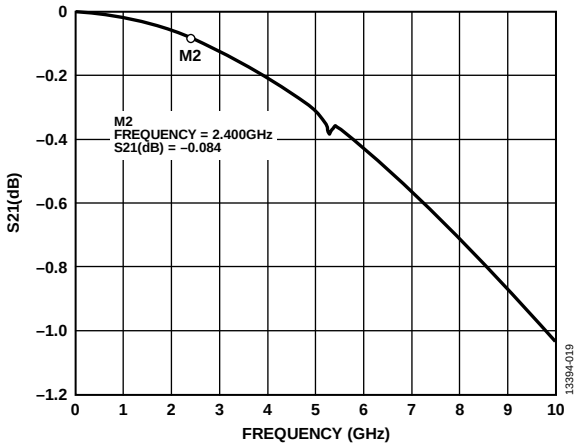

Figure 19. Insertion Loss

Acceptable insertion loss for the PCB layout is less than 1 dB. Maximize the allowable insertion loss of the PCB to optimize the RF performance. Figure 19 indicates that an insertion loss of −0.084 dB has a minimal effect on the power transferred.

Figure 20 shows the corresponding impedance measurements at the feed line of the antenna. The impedance plot on the Smith chart helps determine the tuning necessary to improve the antenna performance at the desired operating frequency.

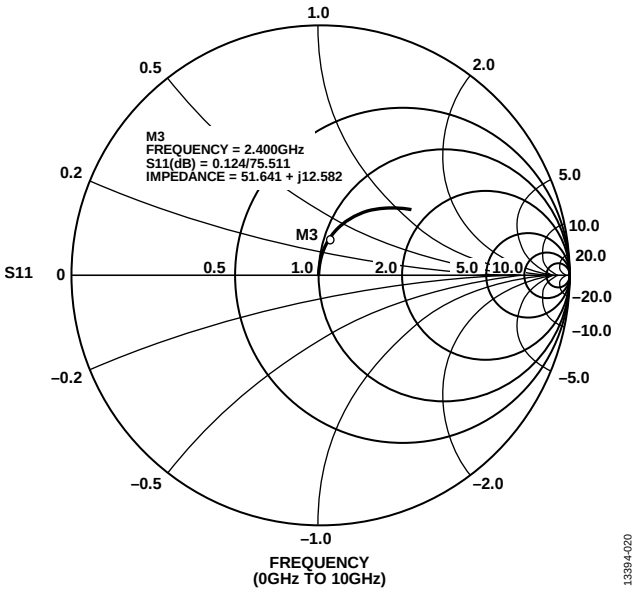

Figure 20. Corresponding Impedance Measurements

CONCLUSION

The design and implementation of the EVAL-ADF7242-PMDZ using a chip antenna was verified by the use of the ADS simulation tool. It is important to determine the RF parameters needed in the simulation, such as return loss, insertion loss, and impedance of the PCB layout, because these parameters greatly impact the actual RF performance of the evaluation board. Proper design of the PCB layout and the RF component results in optimum performance for both the ADF7242 and the 2450AT18A100 chip antenna.

REFERENCES

2450AT18A100 Data Sheet. *Mini 2.45 GHz Antenna.* Johanson Technology, Inc., 2014.

JTI Chip Antenna Mounting and Tuning Techniques, Johanson Technology, Inc.

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